REMARKS

SPECIFICATION

Applicant traverses the Examiner's various objections to the specification.

A substitute specification in proper idiomatic English as revised by the author of the original revised specification translation is provided. No new matter has been introduced.

The substitute specification is based on a newly created translation (translation certification enclosed), revised to provide an improved translation in proper idiomatic English. In addition, the substitute specification has been amended, as indicated in accordance with 37 CFR 1.52(a) and (b).

The present patent application is not concerned with the headings referred to as b), c), d), e) at page 3 of the Office Action.

Consequently relevant headings a), f), g), h), i), j) and k) are introduced within the specification translation to comply with the Examiner's requirements.

In particular, the following headings have been added:

BACKGROUND OF THE INVENTION

Field of the invention

Prior Art

SUMMARY OF THE INVENTION

BRIEF DESCRIPTION OF THE DRAWINGS

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embedded hyperlink references have been deleted.

Trademarks have been capitalized all along the specification translation.

With respect to minor errors in the specification translation or even clerical errors and translation errors a careful checking has been performed so as to introduce the subsequent corrections through out the specification.

Minor and clerical errors:

— Page 21 (marked up version), lines 4, 5 and 6:

The item "ε" which is obviously wrong is corrected to -∈- which clearly defines a symbol introducing the subtyping relationship of inheritance hierarchy between

classes of the applet. See particularly the subtyping relation definition at page 22 from lines 24 to 31 (marked up version).

— Page 34, lines 12, the original mentioned relationship between I_i and AI_i is clearly erroneous. It is thus corrected to read:

$I_i \leftrightarrow AI_i$

in accordance with step 500 of figure 4b, in which the same relation is introduced.

— Page 35 at line 1, the question mark ("?") is clearly erroneous. With reference to step 501 at figure 4a, in which the same relationship between AE and I_i is quoted, the query mark is corrected to ≠.

— Page 37, line 30, the question mark ("?") is erroneous and corrected to ≠ as shown at step 504a of figure 5a.

— Page 38, line 9, the character 3 is corrected to ∃ the existence symbol with reference to step 504 of figure 5a.

Translation errors:

Some translation errors are now corrected, through out the specification and the drawings.

— The term "on-board" is clearly wrong.

With reference to page 1 from line 16 to line 30 relating to the prior art, the dummy "on-board" data-processing systems 10 clearly refers to an -embedded-data- processing systems, as known to any person of ordinary skill in the corresponding art.

Consequently, the term "on-board" of the verified translated specification is corrected to read –embedded- through out the description.

— The term "protocol" which might appear as misleading according to the Examiner's analysis is corrected to -process- all along the description.

The title of the invention is corrected to read:

— A method for transforming and verifying downloaded program fragments with data type restrictions and corresponding system.-

An abstract of the disclosure is attached. A copy of the title page of the corresponding PCT international patent application WO 01/14958 is enclosed for the Examiner's consideration.

DRAWINGS

Applicant traverses the Examiner's objection to the drawings as failing to comply with 37 CFR 1.84 (p)(4).

Reference character 15 is objected to as having been used to designate both an EPROM and a serial link between Fig. 1a.

Referring to the substitute specification translation (marked up copy) at page 2, line 22 the correct reference number for permanent memory is "13", as also shown at Fig. la and lb.

Applicant therefore corrects reference number "15" at page 1 line 21 of the specification translation to -13-, since the objected reference number "15" clearly corresponds to a clerical error only.

Applicant respectfully traverses the Examiner's objection to the drawings under 37 CFR 1.84(p)(5). The following comments and revisions are noted.

— Reference character -13- in relation to Fig 1a is now introduced at page 1, line 21 of the specification translation.

— Reference character "103" of Fig 2 is missing in the specification translation.

The specification translation at page 16, line 19 is corrected by adding reference character -<u>103</u>-.

Missing reference character 103 clearly comes from a clerical error since step 103a and step 103b clearly designate a successful and an unsuccessful response respectively to corresponding verification step, that should have been labeled -103- as shown at figure 2.

— Reference character "306" of Fig 3d is missing in the specification translation.

The item -<u>at 306</u>- at page 25 is inserted between "stack" and "in" to read:

-the verification process reinitializes the type stack <u>at 306</u> in such a way...-

— Reference character 16 of Fig 6 is missing in the specification translation.

Applicant emphasizes that figure 6 clearly refers to Fig lb.

Particularly, Fig 6 is said to disclose an embedded system 10 referred to as 10 that includes the essential components as shown at Fig lb (see particularly the specification translation at page 43 lines 15 to 18) in which item 16 is said to embody a virtual machine 16 (see particularly the specification translation at page 2 from line 24 to line 30).

— Consequently, adding further reference character 16 in relation to Fig 6 will not prove necessary, since the architecture of a reprogrammable embedded data processing system embodying a virtual machine is fully disclosed in the specification and fully know to one or ordinary skill in the corresponding art.

CLAIMS

Applicant respectfully traverses the Examiner's various objections to the claims.

Multidependency of the original claims has been canceled. The amended claims have been recasted to comply with the Examiner's remarks.

The applicant believes that in most cases the lengthy preamble is necessary to explain the invention. Wherever appropriate, the preamble has been split up, as per claims 15, 16 and 22, in which the technical features of the standardized object code which is obtained by applying the method of transforming of the invention are now recited at the end of each corresponding claim. Amending these claims this way will not introduce any new matter, since each claim content is unchanged, while the standardized object code features are now highlighted as the result which is obtained thanks to the claimed method.

Original claims 1-3 have been canceled without prejudice.

Claim 4 is amended and recast by canceling a, b, y headings and introducing corresponding indentation.

Claims 5-6 are amended by canceling the symbols $\perp$ and T. Amending claim 5 and 6 in this manner does not introduce new matter. Underlining within the claims has been omitted. Dashes to delineate steps and/or items are canceled. Bullets points within the claims are canceled.

Claims 1 to 3 are canceled and objection under 35 USC 101 directed to objected claims 1 to 3 is thus overcome.

Moreover, the specification is amended by correcting each occurrence of the item "protocol" to –process-, since, in accordance with the protocol general definition, a protocol is known to concern data exchange among given units, particularly corresponding exchange steps.

Applicant thus believes that the exchange steps better correspond to a process.

Claims 23-25 are rejected, since they are not limited to statutory computer readable media.

Claim 23 has been canceled without prejudice.

Although the computer programs which are the object of the invention are downloaded onto a reprogrammable embedded system, or a system, and thus stored therein, claims 24 and 25 are "A computer program product which is recorded on a medium." Objection under 35 USC 101 is thus overcome.

Rejection of claims 1 to 27 under 35 USC 112 first paragraph is surprising to the Applicant. Although it is agreed that the original claims correspond to a literal translation as requested by the PCT regulation requirements to enter the national phase in the United States, Applicant does not agree that the claim language is an obvious machine translation.

Some of the Examiner's objections appears unfair to the Applicant.

As an example, that "The phrase updating of the effect of said current instructions on the type stack the register table does not ensure that this takes place, thus making the claimed invention boarder than the written description" is technically and judicially unfounded and thus unfair to the Applicant.

Particularly, Applicant refers to the specification translation and corrected version at page 19 from line 25 to line 33 which contain quite the same phrase.

That the claimed invention is broader than the written description as contended by the Examiner is thus traversed.

The Examiner can either accept that the claimed <u>and disclosed</u> updating has taken place and the invention came to reduction to practice, or not.

In the absence of evidences given by the Examiner that reduction to practice did not take place the objection is moot or even unfair to Applicant, in case it would be maintained.

Claims 1-27 are rejected under 35 USC 112 first paragraph for the claimed invention was not described in the specification.

More particularly the virtual machine definition is not sufficient for the invention.

The Examiner's attention is drawn to the specification translation from page 1, line 11 to page 3, line 3.

Applicant believes and strongly emphasizes that the Examiner should be aware that using a virtual machine for interpreting applets within an embedded data-processing system is fully known to any person of ordinary skill in the corresponding art since 1996, as quoted with reference to the Tim LINDHOLM and Frank YELLIN publication at page 2, lines 30 to 55 of the specification translation, while the documentation edited by SUN MICROSYSTEMS Inc. on the JAVACARD 2.1 Virtual Machine Specification was available to every body since March 1999, as quoted at the paragraph spanning pages 2 and 3 of the specification translation.

That the inventor had possession of the claimed invention which is not described in such a way to reasonably convey to one skilled in the art to embody the invention is traversed.

In the absence of evidences given by the Examiner, no evidences are given that the invention was actually not reduced to practice by the inventor(s), the objection is unfounded to the Applicant.

Claims 1 to 27 are rejected under 35 USC 112 second paragraph for they are generally narrative and indefinite.

Amended claims are now recasted to comply with the US practice.

Claims 1-7, 15-19 and 26-27 are rejected under 35 USC 102(b) for they lack novelty over U.S. patent 5,748,964 to Gosling.

Claims 7, 19, 21 and 23 have been cancelled without prejudice.

Although the patent to Gosling is said to meet the object of the invention, Gosling does not perform the verifying method of a fragment project as the method of the invention does.

Particularly, Applicant refers to the specification translation at page 5 from lines 7 to 29 in which the mode of operation of the system as disclosed by the U.S. patent 5,748,964 to Gosling is fully acknowledged and referred to as the third solution, known from the prior art.

Applicant also refers to the International Preliminary Examination Report as established by the International Preliminary Examination Authority and the official translation thereof, of which a copy is provided herewith.

The Examiner's attention should be drawn and made aware of that the object code verifier as disclosed by Gosling, referred to as D1, has the disadvantage of a complex and costly static code verification process both in terms of the code size required to control the processor and in terms of the RAM memory size, as well as in terms of calculation time, with these memory requirements being far greater than the resource capacity of most existing embedded (on-board) computer systems.

In contradistinction to the prior art solution, the invention makes use of a method for standardizing an original object code into a standardized object code with an empty stack branch instruction using typed registers unlike the prior art methods, in which the stack type at every branching target must be stored in memory. The verification method of the invention requires only the type of the execute stack during the instruction execution being verified and does not store the stack type in memory for other subprograms. As a result, the memory capacity requirement is significantly reduced.

More particularly with reference to the substitute specification translation at page 48 line 10 to page 49 line 2, the Applicant further emphasizes that the invention is directed to a novel technique for byte code verification of JAVACARD program fragments, designated as applets, or for program fragments for similar environments.

Basically the verification operation essentially consists in requiring that:

A) the virtual operand stack be empty at each target on a branching instruction, the program fragment being thus rejected if this constraint is not satisfied;

B) the type of the local variables, designated as registers, be identical at all point within a program fragment, designated as a method, the program fragment being thus rejected if this constraint is not satisfied.

Satisfying the above mentioned constraints, in accordance with the method of the invention, allows a very efficient embedded bytecode verifier to be implemented.

As clearly quoted on the preceding highlighted paragraph of the substitute specification translation, for a given program fragment using a maximum stack size of T_p and P_r registers, the memory size required by a byte code verifier according to the invention is a direct proportion to $T_p + P_r$.

By contrast, the verifiers known from the prior art, particularly from the US patent to Gosling, would have required a memory size in a direct proportion to $(T_p + P_r) \times N_b$, the product

of $T_p + P_r$ and the number N_b of targets of branching instructions included within the program fragment.

The invention also concerns a method for transforming any program fragment accepted by any prior art verifier into a program fragment accepted by the bytecode verifier of the invention.

Consequently, while most existing or marketed program fragments or applets would possibly be rejected when submitting them to a verifier of the invention, for these existing or marketed program fragments would not necessarily satisfy the above mentioned constraints A) and B), the invention also implements the method for transforming any existing or marketed program fragment, to be verified and then executed in accordance with the method for verifying of the invention.

The invention, as implemented, appears thus fully useful for any existing or marketed program fragment and does not offend against 35 USC 101 requirements, as contended by the Examiner.

The amended claims are recasted in accordance with the preceding statement by:

- canceling claims 1 to 3, 7, 19, 21 and 23;
- redrafting claim 4 by emphasizing corresponding constraint A) and B) which were explained before.

Remaining amended claims 4, 5, 6, 8-18, 20, 22, 24-27 are thus clearly not anticipated by Gosling and are patentable, since introducing the above discussed constraints so as to allow a significant reduction of the memory size over the most prominent bytecode verifiers of the prior art, particularly these developed by SUN MICROSYSTEMS as disclosed by Gosling, was not known or obvious at the date at which the invention was made;

- recasting claims 20, 22, 24 and 25 as independent claims to cancel reference to another claim of different category.

In view of the foregoing comments and amendment, reconsideration and allowance are requested.

Respectfully submitted,

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